[0016] FIG. **11** shows a top plan view of a wafer of semiconductor material similar to that of FIG. **2**, corresponding to an embodiment of the present invention;

[0017] FIGS. **12** and **13** show cross sections through the wafer of semiconductor material along the line of section XII-XII of FIG. **11** in an initial step and in a final step of the manufacturing process, respectively;

[0018] FIGS. **14***a*-**14***f* show cross sections of a wafer of semiconductor material in successive steps of a manufacturing process of a semiconductor power device, in particular a MOSFET, and of a corresponding edge-termination structure in accordance with a second embodiment of the invention; and

[0019] FIGS. **15***a*-**15***e* show cross sections of a wafer of semiconductor material in successive steps of a manufacturing process of a semiconductor power device and of a corresponding edge-termination structure in accordance with a third embodiment of the invention.

DETAILED DESCRIPTION

[0020] A process for manufacturing a semiconductor power diode with charge-balance techniques is now described according to one or more embodiments of the invention. As will be clarified hereinafter, the structure that is obtained can be used, with the appropriate modifications, to obtain an edge structure for a generic charge-balance power device (for example, a MOSFET, a BJT, etc.).

[0021] FIG. **1** shows a wafer **1** made of semiconductor material, typically silicon, comprising a substrate **2** having a first type of conductivity, for example of an N^{++} type with resistivity lower than 10 mΩ·cm, and an epitaxial layer **3**, also having the first type of conductivity, for example of an N type with resistivity of between 0.1 Ω·cm and 2 Ω·cm. The wafer **1** has, for example, surface orientation <100>, and the epitaxial layer **3** has a top surface **3***a*.

[0022] In an initial step of the manufacturing process (FIGS. **2** and **3**), a first implantation is performed of dopant atoms with a second type of conductivity, in the example a P-type conductivity (with boron atoms), to form a first doped region **4** in the proximity of the top surface **3***a* of the epitaxial layer **3**. As will be clarified hereinafter, the first doped region **4** is to form an anode region of a power diode, and part of a corresponding edge-termination structure (in particular a guard ring). In detail, an implantation is performed with high dose (of between $5\cdot10^{13}$ and $3\cdot10^{15}$ at/cm^2) and medium energy (of between 80 and 160 keV), through a first mask (not illustrated) of appropriate shape, so as to localize the implantation in an active area of the power device and in a perimetral region of the same active area (at the boundary with a corresponding edge region). For example, the first doped region **4** has in plan view a closed generally rectangular shape (as may be seen in FIG. **2**).

[0023] A second implantation of dopant atoms of a P type is then performed through a second mask (not illustrated) to form a ring region **5** of the edge-termination structure of the power device. The implantation, which in the example is also performed with boron atoms, is at a low dose (of between $5\cdot10^{11}$ and $8\cdot10^{12}$ at/cm^2) and high energy (of between 120 keV and 1 MeV). It follows that the ring region **5** is set at a depth lower than that of the first doped region **4** with respect to the top surface **3***a* of the epitaxial layer **3**. In particular, the second mask locates the ring region **5** in the perimetral region of the power device. In detail, the ring region **5** completely surrounds the first doped region **4** and has an area of overlapping **6** with the latter (indicated by the dashed line). It is consequently possible to distinguish in the wafer **1** an active area **1***a*, which is designed for providing active devices (in the example the power diode), and set in which is an active portion **4***a* of the first doped region **4**; and an edge area **1***b*, which is designed for providing an edge-termination structure, and set in which are an edge portion **4***b* of the first doped region **4**, and the ring region **5**.

[0024] Next (FIG. **4**), charge-balance columnar structures **7** are formed through the epitaxial layer **3**, and accordingly also through the already implanted regions, i.e., the first doped region **4** and the ring region **5**, substantially as described in detail in the aforesaid co-pending patent applications WO-PCTIT0600244, and WO-PCTIT0600273.

[0025] In summary, the process for the formation of the columnar structures **7** envisages first the formation, by means of anisotropic dry etching through an appropriate masking, of deep trenches **8** inside the epitaxial layer **3** (and through the first doped region **4** and the ring region **5**). The deep trenches **8** have, for example, a width, at the level of the top surface **3***a*, of between 0.8 and 2 μm and a smaller width at their bottom of between 0.2 and 1.4 μm. In addition, the height of the deep trenches **8** varies, for example, between 5 and 50 μm and determines, together with the thickness of the epitaxial layer **3**, the voltage class of the final device (by way of example, corresponding to a height of 5 μm is a voltage class of 100 V, whereas corresponding to a height of 30 μm is a voltage class of 600 V). Then, the wafer **1** is subjected to an annealing treatment in a hydrogen environment at a temperature of 1000-1150° C. for a treatment time of 1-15 min. This treatment, in addition to eliminating the damage due to the preceding etching, leads to exposure, on the bottom of the deep trenches **8** of the crystallographic planes <100>and <130> and, along the side walls of the plane <010> (the deep trenches **8** consequently assume the shape visible in FIG. **4**). Next, the deep trenches **8** are filled via epitaxial growth with silicon doped with the second type of conductivity, in one example of a P type with boron ions. In particular, the epitaxial growth occurs by supplying a flow of a gas containing silicon (for example, dichlorosilane) and of a gas containing boron (for example, diborane), and the doping control is ensured by maintaining a constant gradient of growth in the flow of diborane (for example, by setting a linear ramp increasing between an initial flow and a final flow of a value twice that of the initial one), and maintaining the flow of dichlorosilane constant. Given that the growth is not selective with respect to the deep trenches **8**, the epitaxial growth is performed both inside the trenches, starting from the side walls, with a faster rate in the proximity of the surface, and outside the trenches, in particular on the top surface **3***a* of the epitaxial layer **3**. In order to prevent premature closing of the deep trenches **8** because of the encounter of the fronts of growth from the walls, successive steps are alternated of epitaxial growth and etching, for example with HCl, of the portions of surface growth (the so-called "multi-step" process). At the end of this process sequence, the structure shown in FIG. **4** is obtained, with the formation of the columnar structures **7**, which completely fill the deep trenches **8** and have a uniform doping spatial distribution and reduced presence of defects (for example, voids). The process of non-selective epitaxial